

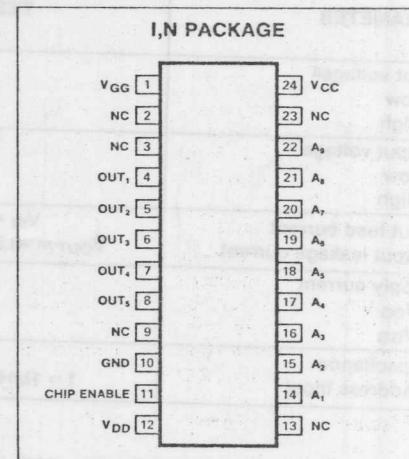
FEATURES

- Standard 7X5 dot matrix fits well
- TTL level interface signals
- Tri-state outputs
- Direct, low cost interfacing with TTL, DTL, CMOS and Signetics MOS 2500 series

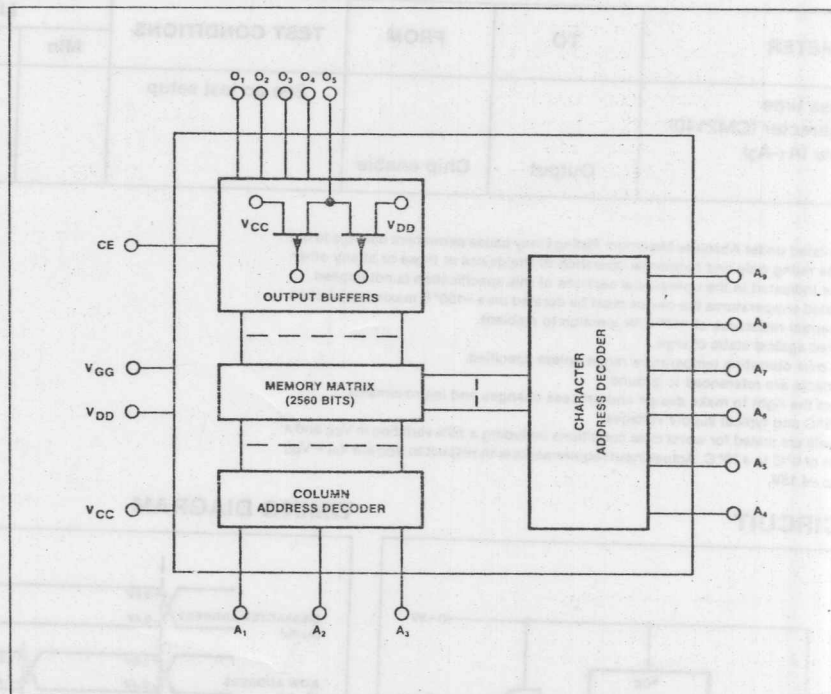
TRUTH TABLE

CE	OUTPUT
0	Data
1	Open

PIN CONFIGURATION



BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
TA	Temperature range	°C
TSTG	Operating	0 to 70
	Storage	-65 to 150
PD	Power dissipation at TA = 70°C ²	730
	Input3 and supply voltages with respect to VCC	0.3 to -20
		mW
		V

DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$,
 $V_{GG} = -12V \pm 5\%$ unless otherwise specified. 4,5,6,7

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} V_{IH}	Input voltage ⁸ Low High			0.6 5.3	V
V_{OL} V_{OH}	Output voltage Low High			0.4	V
I_{LI} I_{LO}	Input load current Output leakage current		10 10	500 1000	nA nA
I_{DD} I_{GG}	Supply current V_{DD} V_{GG}		12 10	15 25	mA
C_{IN}	Capacitance Address input			10	pF

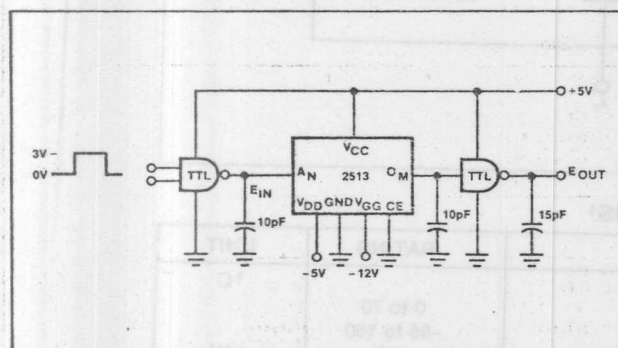
AC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$,
 unless otherwise specified.

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
t_{CA} t_{RA} t_{CE}			See ac test setup		500 450 150	600 500	ns

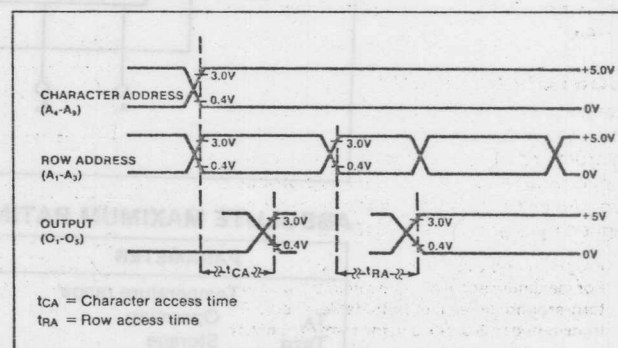
NOTES

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
- For operating at elevated temperatures the device must be derated on a $+150^\circ\text{C}$ maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
- All inputs are protected against static charge.
- Parameters are valid over operating temperature range unless specified.
- All voltage measurements are referenced to ground.
- Manufacturer reserves the right to make design and process changes and improvements.
- Typical values at $+25^\circ\text{C}$ and typical supply voltages.
- Guaranteed input levels are stated for worst case conditions including a $\pm 5\%$ variation in V_{CC} and a temperature variation of $0^\circ\text{C to } +70^\circ\text{C}$. Actual input requirements with respect to V_{CC} are $V_{IH} = V_{CC} - 1.85V$ and $V_{IL} = V_{CC} - 4.15V$.

TEST LOAD CIRCUIT



TIMING DIAGRAM



- **Programming with punched cards:**
For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.

CARD FORMAT

[illegible]

ASCII CHARACTER FONT

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ABOUT CHARACTER FONT

For more information, please visit our website.